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FIG. 1

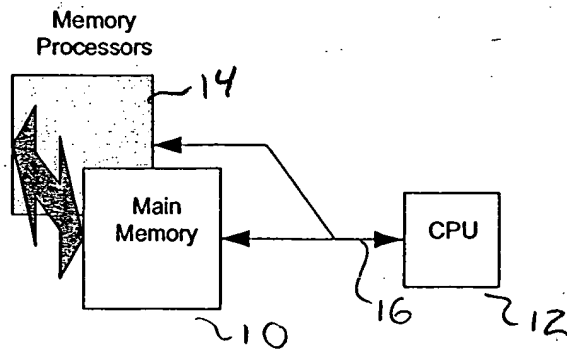
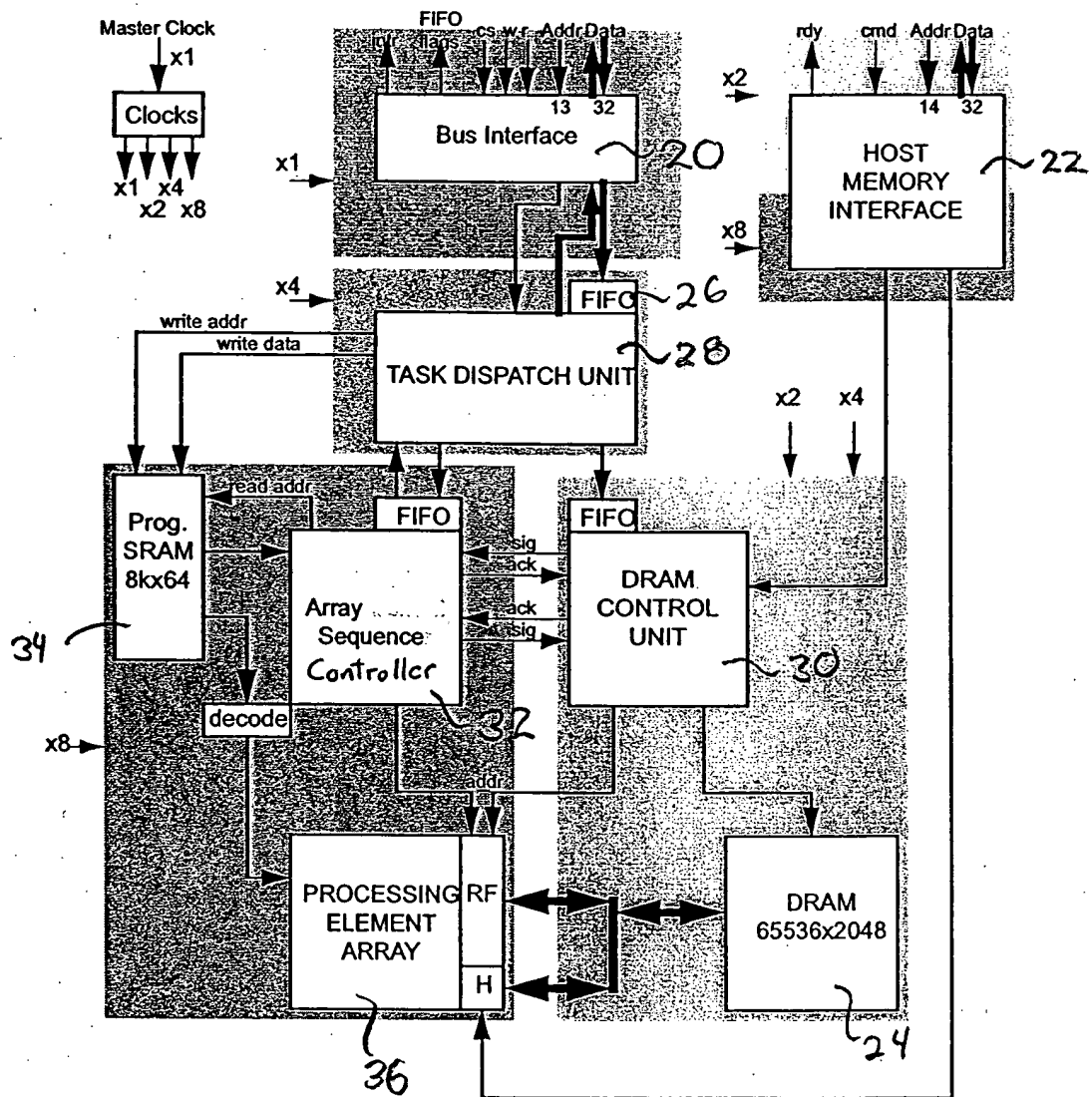
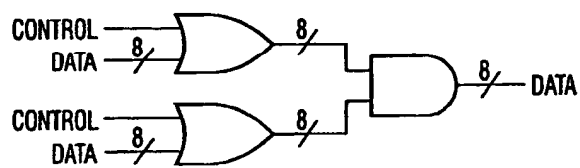
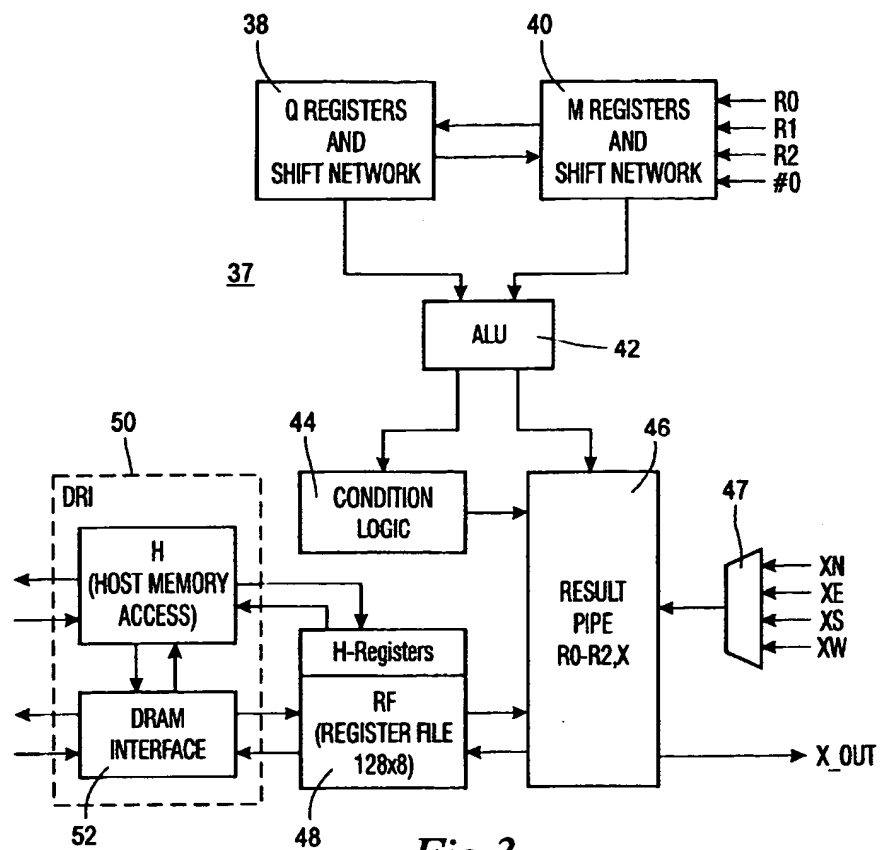
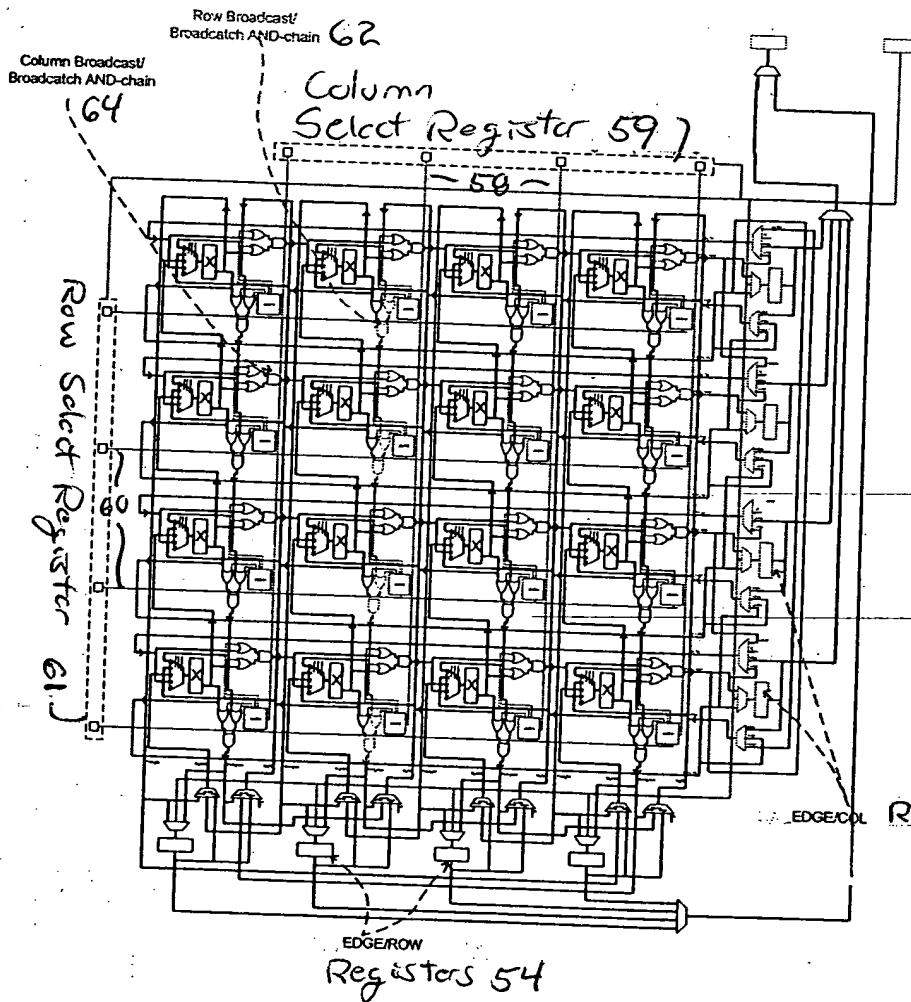


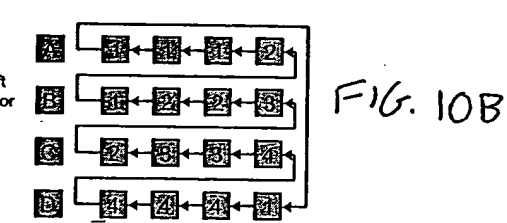
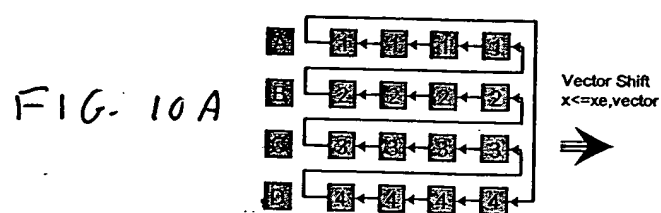
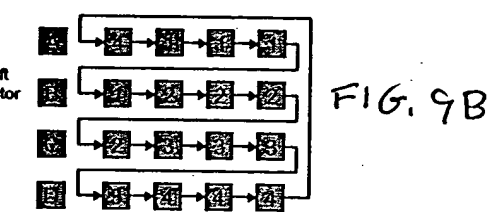
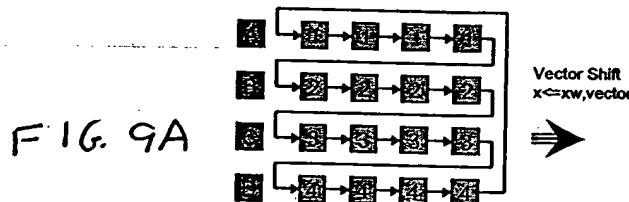
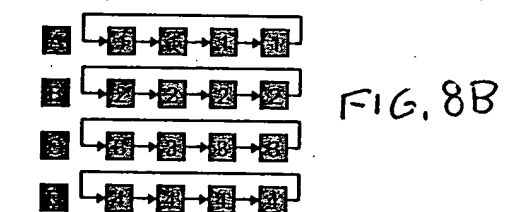
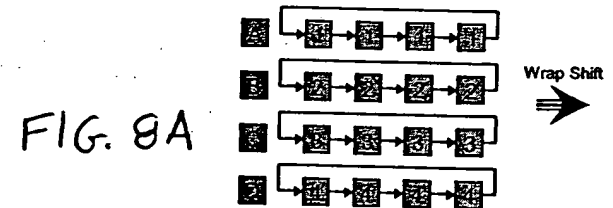
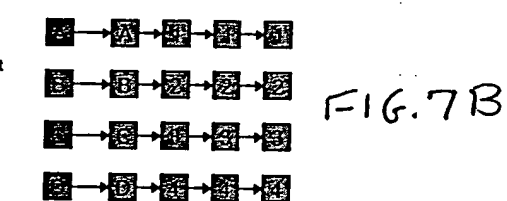
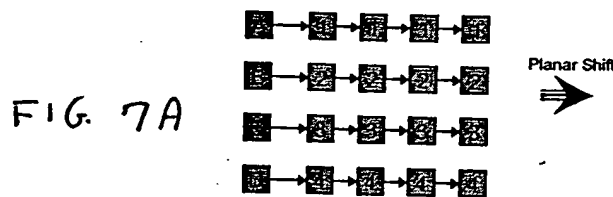
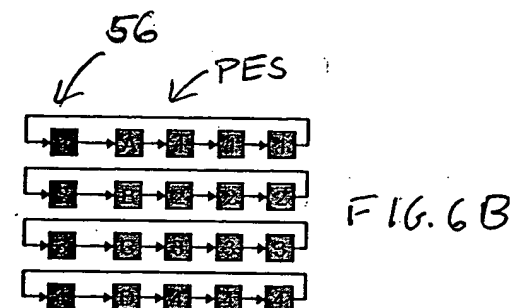
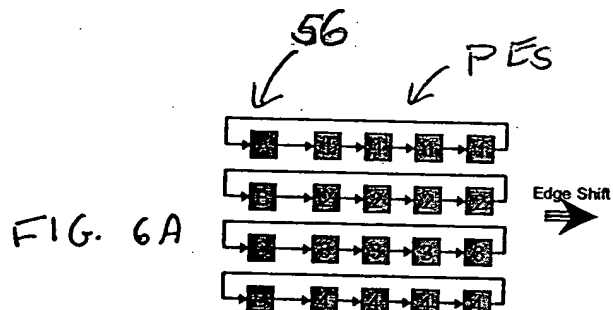
FIG. 2





Data registers  
from 10 32





Data is broadcast from edge registers

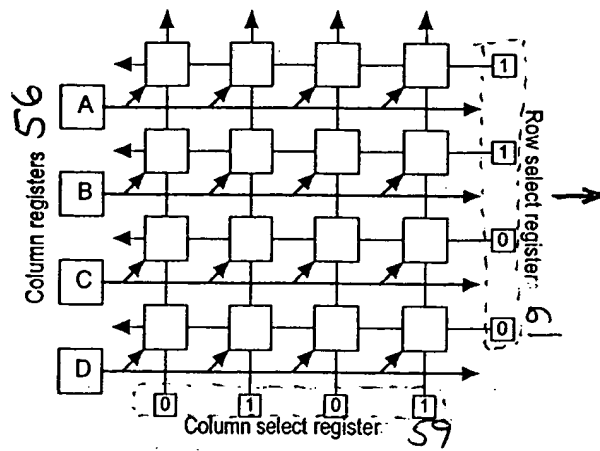


FIG. 11A

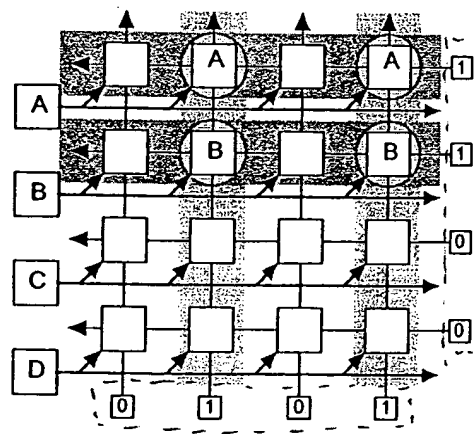


FIG. 11B

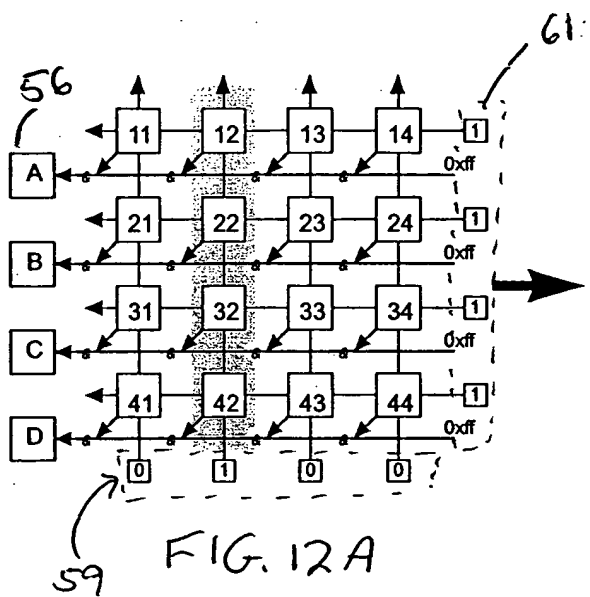


FIG. 12A

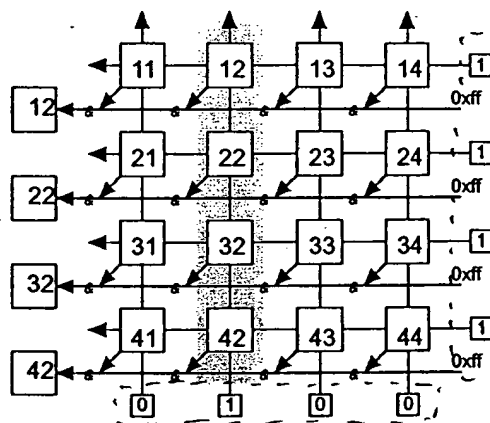


FIG. 12B

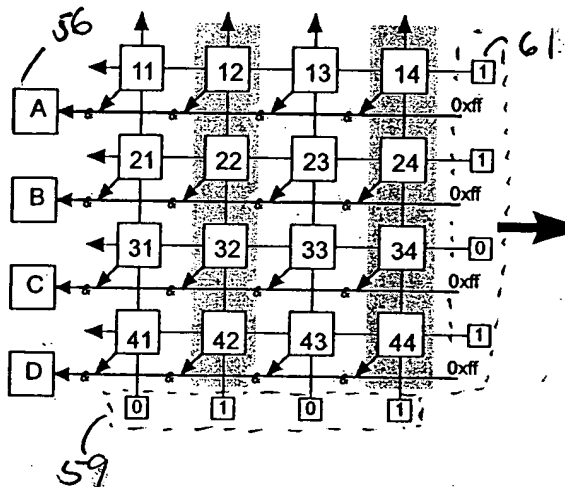


FIG. 13A

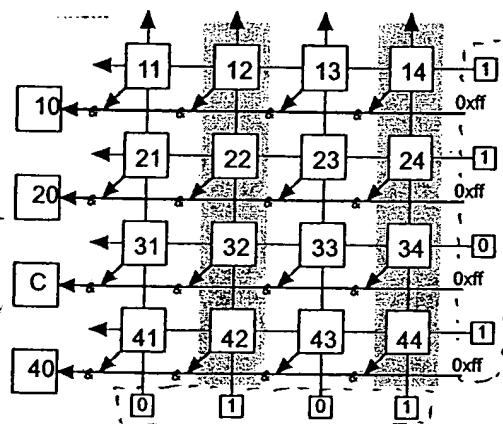


FIG. 13B

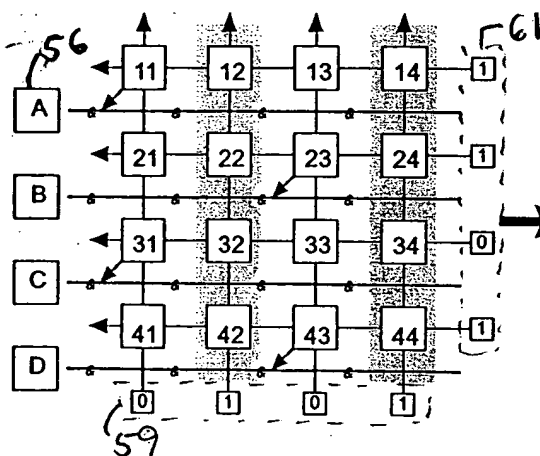


FIG. 14A

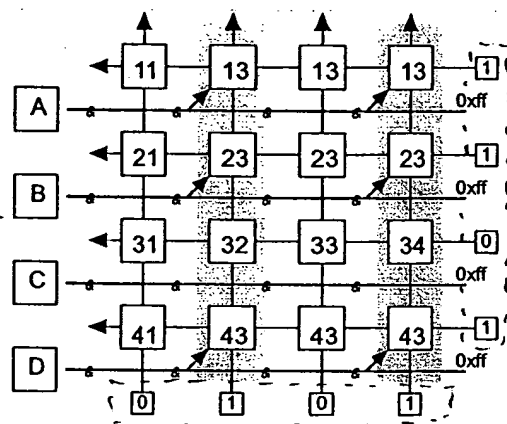


FIG. 14B

C7 C5 C3 C1  
C6 C4 C2 C0

r0	A0	A1	A2	A3	A4	A5	A6	A7
r1	B0							B7
r2	C0							C7
r3	D0							D7
r4	E0							E7
r5	F0							F7
r6	G0							G7
r7	H0	H1	H2	H3	H4	H5	H6	H7

FIG. 15A

[illegible]

FIG. 15B

B9			A7	B7	C7	D7	E7	F7	G7	H7
	C6		A8	B8	C6					H6
		D5	A5		C5	D5				H5
			A4			D4	E4			H4
			A3				E3	F3		H3
			A2					F2	G2	H2
			A1						G1	H1
			A0	B0	C0	D0	E0	F0	G0	H0

FIG. 15D

B7	C7	D7	E7	F7	G7	A7	A7
C6					H6	A6	B6
D5				H5	A5		C5
E4			H4	A4			D4
F3		H3	A3				E3
G2	H2	A2					F2
H1	A1						G1
A0	B0	C0	D0	E0	F0	G0	H0

FIG. 15C



A0	A1	A2	A3	A4	A5	A6	A7
B0							B7
C0							C7
D0							D7
E0							E7
F0							F7
G0							G7
H0	H1	H2	H3	H4	H5	H6	H7

FIG. 16A

A0	A1	A2	A3	A4	A5	A6	A7	A0	A1	A2
B0								B7	B0	B1
C0								C7	C0	
D0								D7		
E7	E0							E6	E7	
F6	F7	F0						F5	F7	
G5	G7	G0						G4		G7
H4	H5	H6	H7	H0	H1	H2	H3	H4	H5	H6

FIG. 16B

E7			A7	B7	C7	D7	E7	F7	G7	H7
F6			A6				E6	F6		H6
G5			A5				F5	G5		H5
H4			A4				G4	H4		
			A3				H3			
			A2	B2			H2			
			A1	B1	C1		H1			
			A0	B0	C0	D0	E0	F0	G0	H0

FIG. 16D

										A2
										A1
										A0
E7	F7	G7	H7	A7	B7	C7	D7			
F6		H6	A6				E6			
G5	H5	A5					F5			
H4	A4						G4			
A3							H3			
B2							H2	A2		
C1							H1	A1	B1	
D0	E0	F0	G0	H0	A0	B0	C0			

FIG. 16C